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FPGA-based Model Predictive Dynamic Navigation for Indoor Deployment of UAVs

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***Abstract*—This study proposes a high-speed FPGA-based flight control unit (FCU) with integrated model predictive control (MPC) for improved real-time flight planning and obstacle avoidance in indoor environment. Initial results demonstrate successful FCU implementation and ongoing experiments to evaluate indoor navigation performance.**

***Index Terms*—Model Predictive Control, Field Programmable Gate Array, Unmanned Aerial Vehicles, Flight Control Unit, Collision Avoidance.**

I. Introduction

Indoor UAV navigation poses distinct challenges, such as confined spaces and moving obstacles [1]. Although employing model predictive control (MPC) for flight path planning and obstacle avoidance is a promising solution to this problem, its real-time implementation is hindered by the limited computational capacity.

Past research has utilized onboard mini-computers to implement MPC for drone navigation, achieving a prediction update frequency of 2 Hz [2]. However, such setup requires a safety distance of 5 meters, which is inadequate for narrow indoor environments. To further reduce the safety distance, it is necessary to further increase the MPC update frequency, necessitating faster optimization computations.

Several high-speed FPGA-based MPC solvers are available [3]. These FPGA implementations can attain MPC prediction update frequencies surpassing several kilohertz at equivalent problem complexities. However, the current ARM-based flight control unit (FCU) does not integrate with FPGA technology. Thus, this study aims to design an FPGA-based flight control unit and integrate both low-level flight control and MPC on FPGA to achieve high-frequency indoor flight navigation.

II. System Architecture

The computational architecture of the proposed FPGA-based FCU using the Zynq UltraScale+ system-on-chip is illustrated in Fig. 1. An onboard camera is used to capture visual feedback. Obstacle information is then processed by the navigation planner to create system constraints. MPC optimization generates optimal drone position commands. These commands are then sent to the low-level flight control, which controls the drone's four rotor speeds.

III. Preliminary Results

The low-level flight control using the proposed FPGA-based FCU has been implemented (Fig. 2). Additionally, the MPC formulation and solver have been incorporated into the FPGA. We are presently conducting flight control experiments to assess navigation performance in indoor environments.

References

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Fig. 2. Hovering test of low-level flight control. The red circle indicates the location of the FPGA-based FCU.

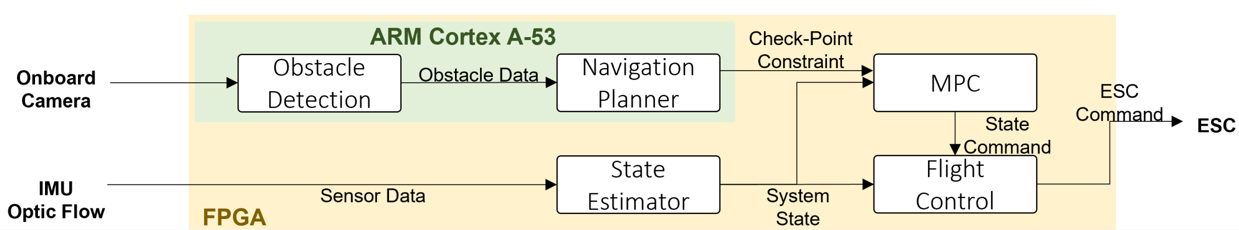

Fig. 1. Computational architecture of the proposed FPGA-based Flight Control Unit (FCU) using the Zynq UltraScale+ system-on-chip. MPC and low-level controllers are placed on the FPGA PL part. Image processing and MPC constraint generation are placed on the PS part (on-chip ARM processor).

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